Synnix™

Chip Card Interface STD100

Feature:

- Interfaces for serial bus or I^2C bus
- Specification compliant with ISO7816, EMV and PC/SC
- Compliant with Microsoft Plug & Play COM device 1.0
- Data Encryption Algorithm compliant with ANSI X9.52 /FIPS PUB 46-3
- Read /Write ISO 7816 asynchronous smart card T=0 /T=1 protocols
  - PTS management
  - Direct/inverse conversion
  - Different communication rate
  - IFSD adjustable
  - Full function of S-block: Resynch, WTX, Abort, IFS
- Support up to 6 smart card slots, including 5 slots for SAM.
- Built-in internal flash memory for software upgrade
- Built-in DES/3DES engine
- Serial interface baud rate to host system: software programmable from 9600 to 38400bps
- Power-saving mode
- 44 pin PQFP package

Application:

- Security & Identification
- E-Commerce
- Banking & Payment
- Gaming & Education
- Access control
- P.O.S & Terminals
- Telecommunication
- Transport
- ATM

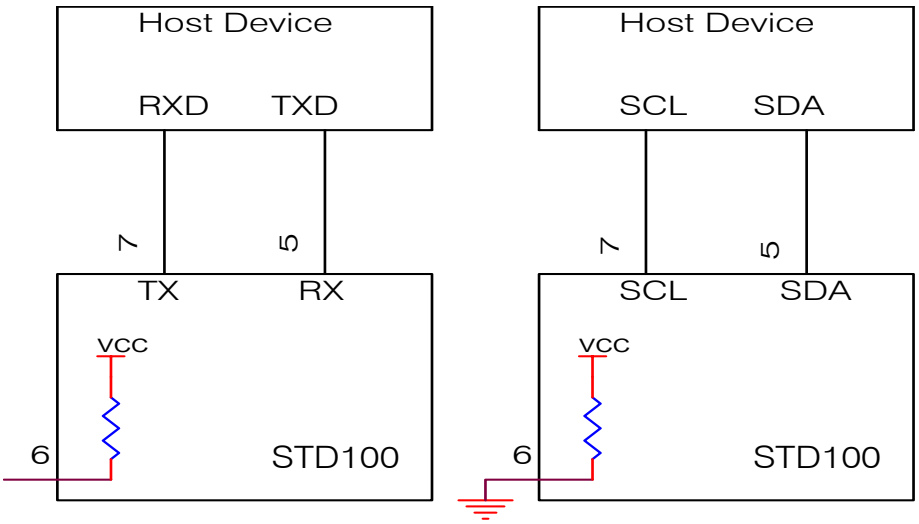
The STD100 was developed to provide the designer with a single multi-function device offering a flexible and easy way to connect to the smart cards. By using the STD100, the designer eliminates the task of assuring ISO 7816, EMV and PC/SC specification compliance and the necessity of understanding smart card timing requirements when interfacing a smart card application.

Communication Interface

The communication interface between the STD100 and host system can works either through a standard serial interface or an I^2C bus determined by opening or tied the IF_SEL pin to ground during the hardware-reset period.

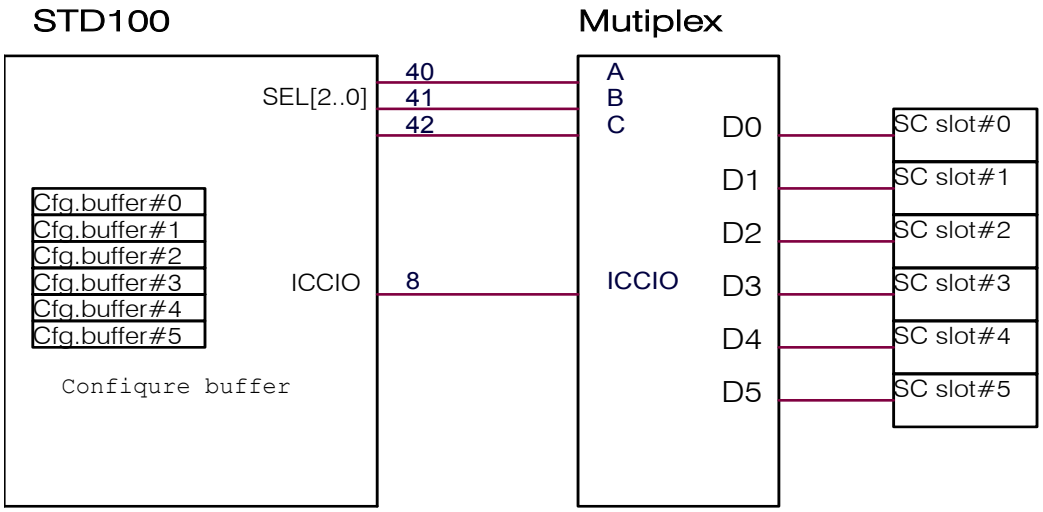
The standard serial interface was chosen if IF_SEL pin is kept open in the power-on reset period. The default protocol will be used to communicate with host system via RX and TX line all the while, until the STD100 receives the Change Protocol command from host system. See User's manual for detail information.

The I^2C bus interface was chosen in the power-on reset period, if IF_SEL pin is tied to ground. The SDA and SCL will transit data instead of RX and TX line.



Multiple Smart Card Slots

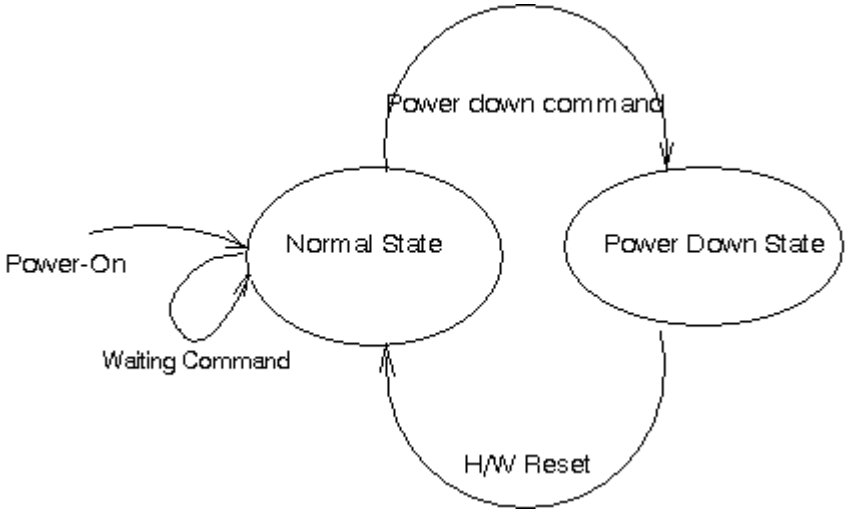
The STD100 supports multiple smart card slots for wide applications; all smart cards share one I/O line to communicate with STD100 via external analog switch. Up to six smart cards can operate with STD100 concurrently, the six regions memory inside the STD100 keep corresponsive parameters that comes from smart cards in each slots. The chip calculates the ATR that is sent form smart card in each slot, and then stores these parameters to corresponsive memory regions. Once the every command comes form host system, the STD100 interprets this command and transfer to electrical signal to communicate with smart card determined by these parameters. These parameters contain F, D, I, P, N, CWT, BWT… etc.



● Power Management

For applications where power consumption is critical the STD100 provides power-reduced state of operation. The STD100 operates two states, Normal operation states, and Power-Down state. After the power-on reset, this chip is running in the Normal state. In this state, it always waits the command inputting from host system. Once the Power-Down command was received and responding status without error was returned to host system, it means that Power-Down action is recognized by chip, the chip will goes into Power-Down state immediately.

In the Power-Down state of operation, VCC can be reduced to as 2.5V, Care must be taken, however, to ensure that VCC is not reduced before the Power-Down state is invoked, and that VCC is restored to its normal operating level, before the Power-Down state is terminated.
The only way to exit from Power-Down state is a hardware reset. After hardware reset, the previous setting of this chip is still contained. Host system keeps the previous protocol setting to communication without any re-configure. A recovery time is required when the chip wake up form Power-Down state via hardware reset. (Approximate 300msec)



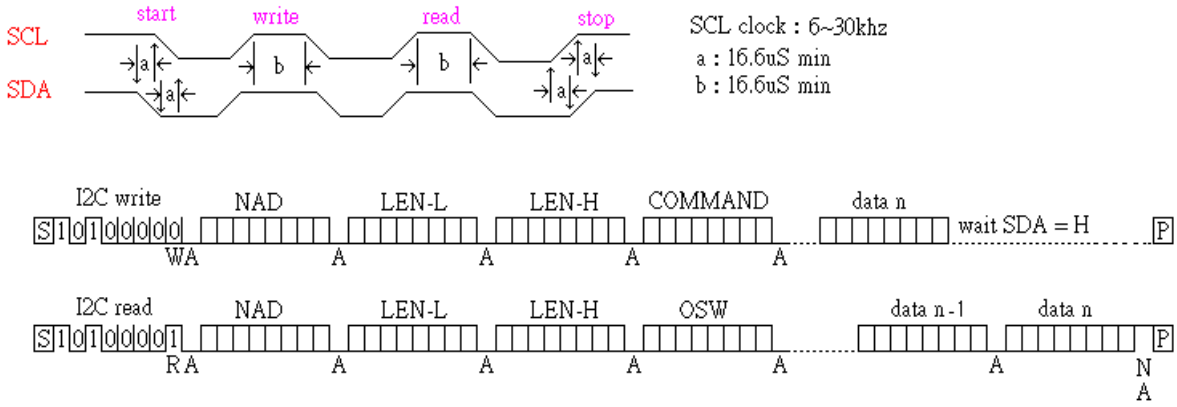
State Diagram

Programming mode

The soft upgrading is provided by the STD100 via commands. This advanced feature offering an easy way to upgrading the firmware inside the chip eliminates the task of changing hardware and save much maintenance's cost if any specification was changed or adds more functions.

I²C Interface

The timing of the I²C bus is described below, note that adds the A0 or A1 command before the access this device.



STD100 Pin Description

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Pin No	Signal	Type	Descriptions
38,29	VCC	P	Supply voltage.
16	VSS	P	Circuit ground.
15	XTAL1	I	Input to the inverting oscillator amplifier and the internal clock generate circuits. To drive the device from the external clock source, XTAL1 should be driven, while XTAL2 is left unconnected.
14	XTAL2	O	Output from the inverting oscillator amplifier
4	RESET	I	A high level on this pin for 2 μs while the oscillator is running resets the device.
26,27,31,30, 17,39,28,25	X		For factory use only. Must be left open.
6	IF_SEL	I	Interface bus selection, when I^2C bus is selected, this pin must tied to low before power on. When serial bus is selected, keep this pin open before power on.
7	TX/SCL	O I	Transmitter data output, if serial bus is selected. Clock line if I^2C bus is selected.
5	RX/SDA	I I/O	Receiver data input, if serial bus is selected. Data line if I^2C bus is selected.
43,44	I_PWR_CTRL0# | I_PWR_CTRL1#	O	ICC power control pin for slot 0~1. This pin is used to enable/disable ICC power for slot 0~1.
1	I_PWR_CTRL2#	O	ICC power control pin for slot 2 ~ 5. This pin is used to enable/disable ICC power for slot 2 ~ 5.
37,36,35, 34,33,32	ICC_RST0# | ICC_RST5#	O	ICC reset pin 0~5. This pin is used to reset ICC for slot 0~5. This output pin is an open-drain.
18,19,20, 21,22,23	ICC_DET0# | ICC_DET5#	I	ICC detecting. This pin is use to indicate ICC is present at slots or absent.
8	ICC_IO	I/O	This pin is used to receive/transmit data from/to smart card.
11,10	CLK_STP0# | CLK_STP1#	O	This pin is used to stop ICC clock for slot0~1.
24	CLK_STP2#	O	This pin is used to stop ICC clock for slot2~5.

40,41,42	SEL0# | SEL2#	O	Smart card slot selection: SSEL [2..0]=000, Select slot 0 SSEL [2..0]=001, Select slot 1 SSEL [2..0]=010, Select slot 2 SSEL [2..0]=011, Select slot 3 SSEL [2..0]=100, Select slot 4 SSEL [2..0]=101, Select slot 5
2	PWR_DOWN#	O	Power down indicator. If this chip goes into the power down state by power down command, this pin will transit to low level until hardware reset is occurred.
3	LED_CTRL	O	LED display control. This pin is used to indicate the device operation. In normal mode, it keeps high state 1second and low state 1second repeating when this chip is waiting for command input.
9	ERR_DET#	I	Error detection. An active low signal forces all ICC signal to go into de-active state.
12	PnP_DTR	I	Plug & Play signal detection. This pin is used to detect PnP signal through DTR from serial port.
13	PnP_RTS	I	Plug & Play signal detection. Detect PnP signal after the correct PnP signal was received. This pin is connected to the RTS from serial port.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Ambient temperature under bias	0	70	^{0}C
Storage temperature	-40	150	^{0}C
Voltage on VCC pin with respect to GND	-0.5	6.5	V
Voltage on any pin with respect to GND	-0.5	VCC +0.5	V
Input current on any pin during overload condition	-10	+10	mA
Absolute sum of all input current during overload condition	100mA		

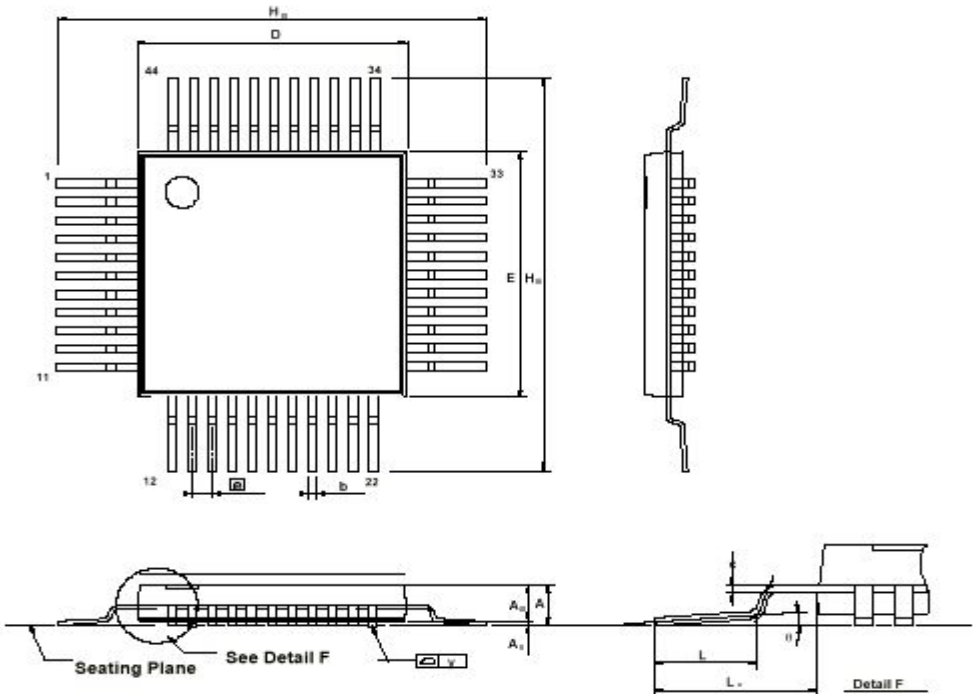
DC Characteristics

DC Characteristics for STD100 Ta= 0 - 70° C, GND= 0V, VCC = 5V±10%

Symbol	Parameter	Min	Max	Unit	Test condition
V_{IL}	Input Low Voltage	-0.5	0.2 Vcc-0.1	V	
V_{IL1}	Input Low Voltage(RESET)	-0.5	0.2 Vcc+0.1	V	
V_{IH}	Input High Voltage	2.7	Vcc +0.5	V	
V_{IH1}	Input High Voltage (XTAL1)	0.7Vcc	Vcc +0.5	V	
V_{IH2}	Input High Voltage (RESET)	0.6Vcc	Vcc +0.5	V	
V_{OL}	Output Low Voltage	-	0.45	V	I_{OL}=1.6mA
V_{OL1}	Output Low Voltage (O.D. pin)	-	0.45	V	I_{OL}=3.2mA
V_{OH}	Output High Voltage	2.4 0.9 Vcc		V	I_{OH}=-80μA I_{OH}=-10μA
V_{OH1}	Output High Voltage (O.D. pin)	2.4 0.9 Vcc		V	I_{OH}=-800μA I_{OH}=-80μA
I_{IL}	Logic 0 input current		-75	μA	Vin=0.45V
I_{TL}	Logic 1-to-0 transition current		-650	μA	Vin=2V
I_{LI}	Input leakage current	-	+10,-10	μA	0.45<Vin<Vcc
$C_{I/O}$	I/O Capacitance		10	pF	Fc=1 Mhz Ta=25^{0}C
Icc	Power supply current	Operation	25	mA	Vcc =5V
		Power down	150	μA	

Package Information:

QFP-44 pin



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.